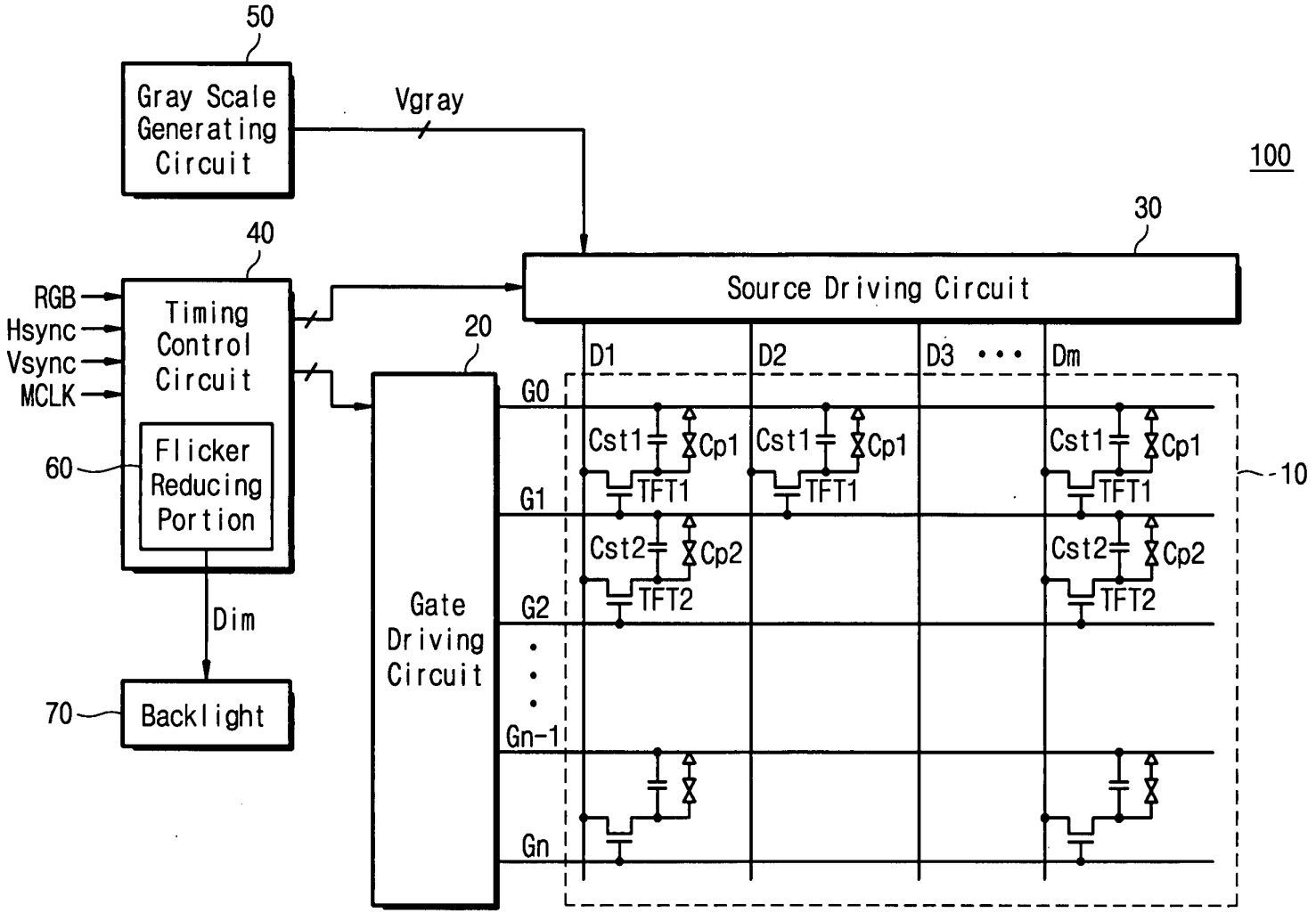
Fig. 1


50
Gray Scale Generating Circuit
Vgray
100
30
40
Source Driving Circuit
RGB
Hsync
Vsync
MCLK
Timing Control Circuit
20
D1
D2
D3 • • •
Dm
G0
G1
G2
Gn-1
Gn
Cst1
Cp1
TFT1
Cst2
Cp2
TFT2
10
60
Flicker Reducing Portion
Dim
Gate Driving Circuit
70
Backlight

1020040095690

Fig. 2

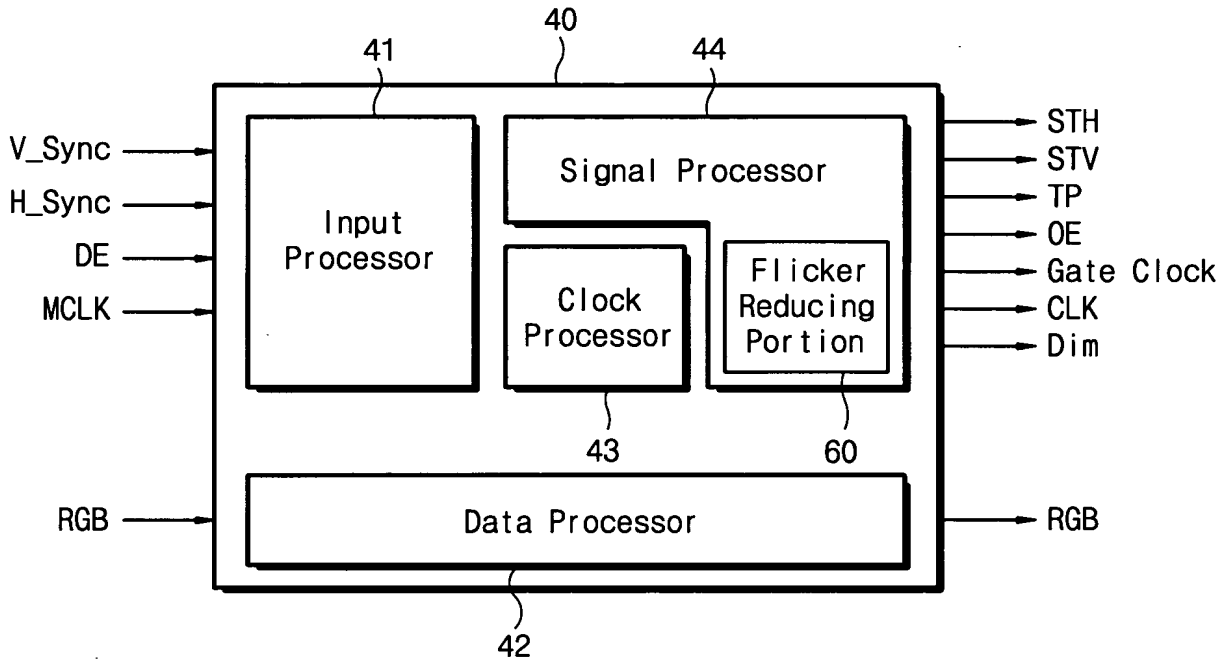


Fig. 3

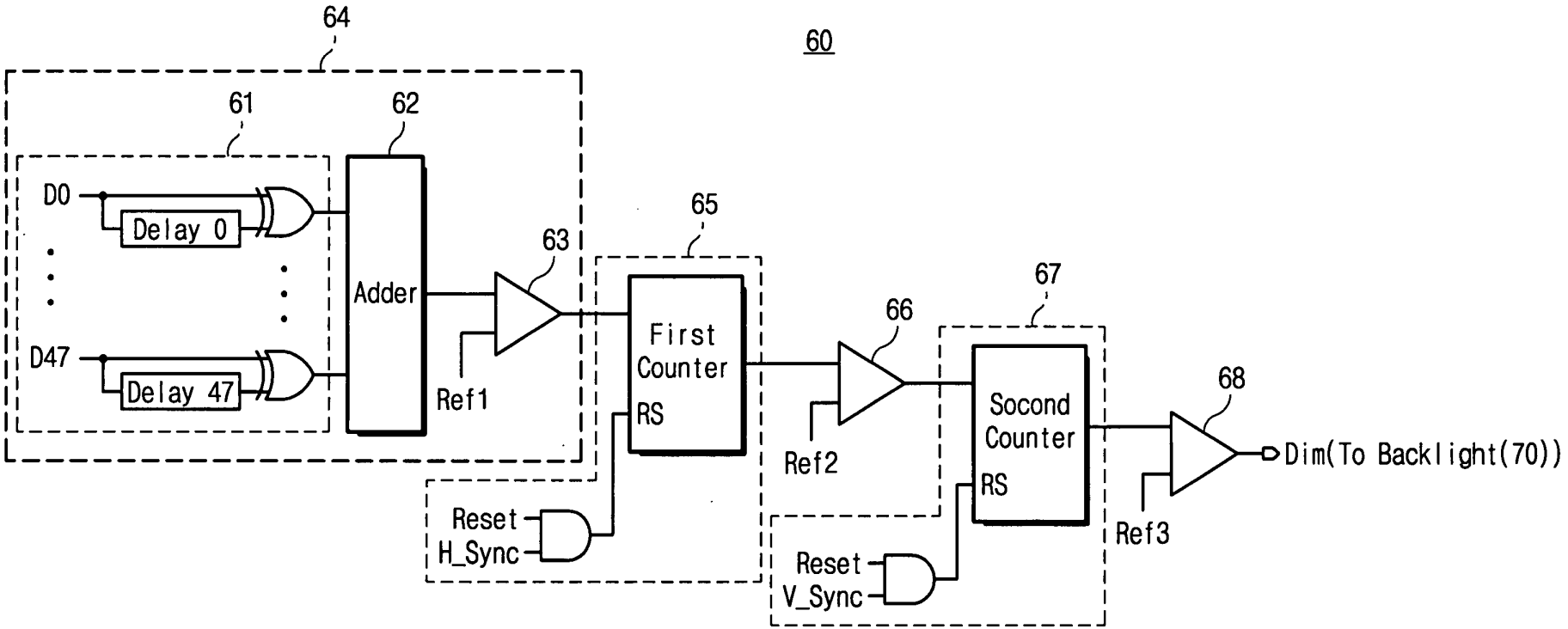
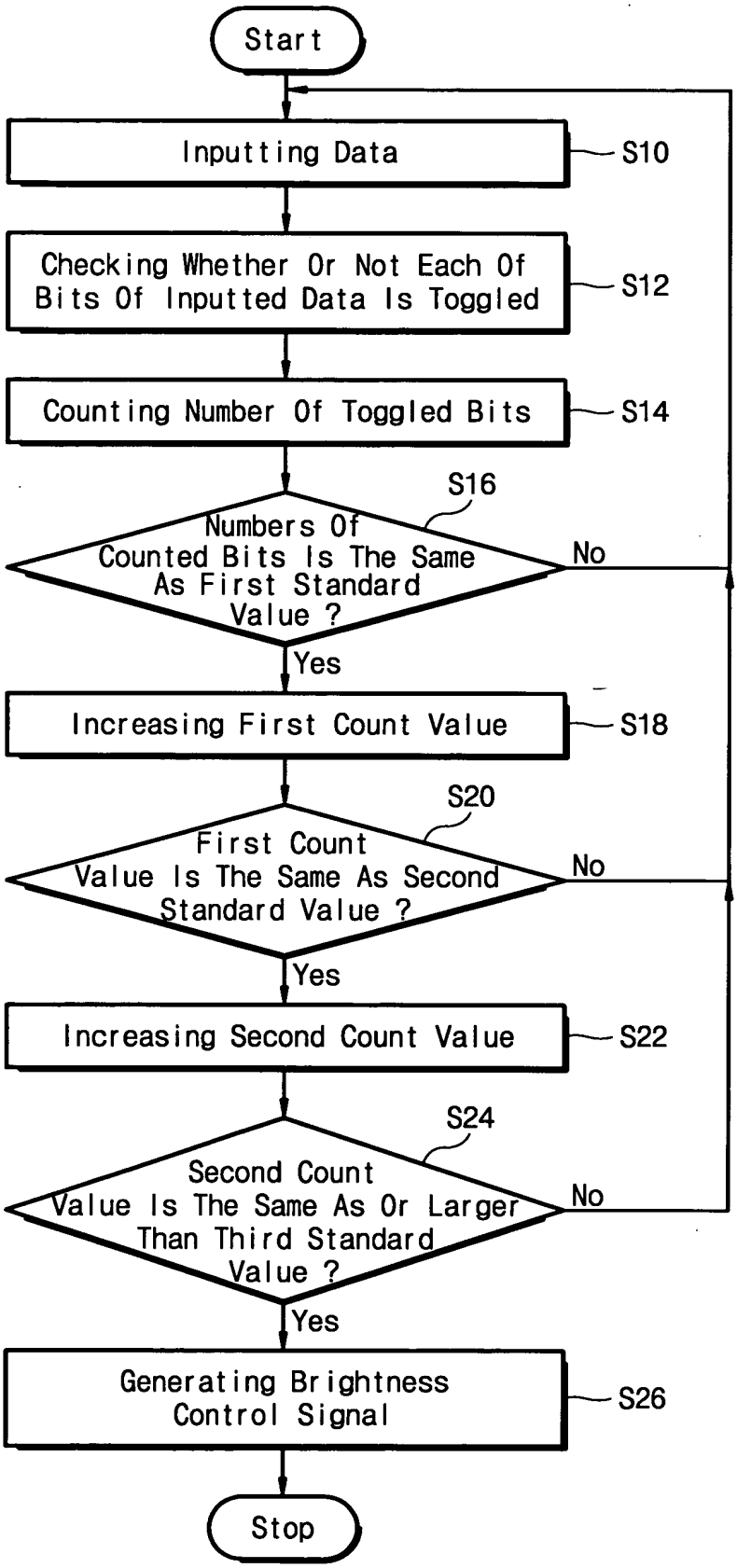

64
60
61
62
D0
Delay 0
D47
Delay 47
Adder
63
Ref1
65
First
Counter
RS
Reset
H_Sync
66
Ref2
67
Socond
Counter
RS
Reset
V_Sync
68
Ref3
Dim(To Backlight(70))

Fig. 4



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